Andreas Schulz

Profession: Consulting Engineer
Freelancer

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BACKGROUND SUMMARY

I am a design & layout engineer with over 16 years of experience in backend activities, such as floorplanning, top-level chip integration, layout finishing, IR drop, physical verification and more.

Throughout these years I was actively involved in more than 30 silicon tape-outs in different technologies ranging from 180 nm to 45 nm. Most of these designs are utilized in automotive industry applications, where zero defect ratio is required.

I have participated in international safety design projects in the past, where many additional tighter design requirements are dictated by the safety standards.

In the last year I was able to expand my skills in Full Custom Layout for various high-voltage components.

PROFESSIONAL EXPERIENCE

Since 2015 **Custom Layout Engineer**
Freelancer
Layout, IGBT
Infineon, Munich

- Layout IGBT's and Verification (DRC)
- Scripting, Diva Rule Writing and Extraction
- Fab Order and Data/Mask review

2012 - 2015 **Physical Design Engineer**
Freelancer
BU-ID, Backend
NXP, Hamburg

- Bonding checks (pad placement, packages, verification)
- Chip size estimations, design floorplanning, macro placement
- Power planning, power grid and analog/special routing
- Implementation of Security & Safety Features, Design Reviews
- Initial Place & Route, congestion analysis, timing closure (asyn. design)
- Chip finishing, Layout generation, static & dynamic IR drop analysis
- Writing and optimization of TCL scripts (FE), Makefiles
- Physical Verification (DRC, LVS, ANT, ERC, DFM, Safety checks)

2011 **Physical Implementation Engineer**
Freelancer
Backend, Layout
Fujitsu, Langen/Munich

- IO Frame generation and validation, bonding checks
- Power planning, optimization, power grid and power domain implementation, analog routing and resistance calculations
- Design floorplanning, analog and digital macro placement
- Initial Place & Route, congestion analysis
- Physical Verification (DRC, LVS, ERC, ANTENNA checks)
- Early Rail Analysis (ERA)
- Writing, running and optimization of scripts for above tasks
- SubVersion (Revision Control System)

2001 - 2010 **Design & Layout Engineer**
Backend, Chip Creation, 32-bit Microcontroller
Freescale/Motorola, Munich

- Floorplanning activities
  - Integration of analog and digital Hard IPs
  - Routing of power and special nets
  - Early timing analysis after placement
  - Static IR drop analysis and improvements
- Design for manufacturability (DFM) analysis and improvements
- Chip finishing activities
  - Generation of final top-level layout (ready for tape-out)
  - DRC and LVS checks (responsibility for physical verification)
  - Mask data preparation and review
- Evaluation of different CAD tools for floorplanning and physical verification
- Experienced in managing project data with DesignSync

1998 - 2000 **Design Support Engineer**
Backend, Multi Media Design Center
Motorola, Munich

- CAD tools support and installation
- ClearCase support and project administration
- Layout verification (DRC and LVS)
- Programming knowledge in PERL, TCL and UNIX shell scripting
- Experience with MySQL databases and their administration
- Web administration (Apache Server) and programming PHP/HTML
- Archiving of project data and documentation

EDUCATION

1990 - 1997 **Degree Course Electrical and Communications Engineering**
FH Braunschweig-Wolfenbüttel

Paused 2 years for further financing of Study
Degree: Dipl.-Ing. (FH) Communications Engineer
Final Grade: 2

1989 - 1990 **Technical College**
Braunschweig

1986 - 1989 **Industrial Education as Communication Technician**
ANT Nachrichtentechnik (Siemens AG), Braunschweig

1975 - 1986 **Elementary and Middle School**
Remlingen/Wolfenbüttel

PROFESSIONAL TRAININGS (Overview of the last 10 years)

- Mentor Graphics
  - Calibre User Training, Newbury, England
  - Calibre Viewing Tools (Update), Munich
  - Calibre Rule Writing, Munich
- Cadence
  - Virtuoso Layout - Chip Integration Flow, Haar
  - First Encounter Training, Feldkirchen
  - Low Power Implementation, Hamburg (2014)
  - NanoRoute Training, Feldkirchen
  - Common Power Format - Coding Training, Feldkirchen
  - Design Framework II Installation and Usage, Haar
- Programming in TCL, Munich
- PERL Scripting, Munich
- DesignSync (MatrixOne) User Introduction, Munich
- ClearCase (IBM) User and Admin Training, Munich
- Unix (Sun) Solaris User and Admin I Training, Haar

TECHNICAL SKILLS

Scripting/Programming languages

- PERL, 6 years
- TCL, 8 years
- VHDL, 1 year
- UNIX shell scripting, 12 years
- HTML, PHP, MySQL, 10 years
- C, Assembler, Pascal, 2 years

CAD tools

Cadence

- Virtuoso (layout editing, chip finishing), 10 years
- Encounter (floorplanning activities), 12 years
- NanoRoute (place and route), 5 years
- Voltage Storm, EPS (IR drop analysis), 2 year
- Space Based Router (special routing), 1 year
- PVS, Assura, Dracula (DRC and LVS), 6 years

Mentor Graphics

- Calibre (DRC and LVS), 12 years

Apache

- RedHawk (IR drop, static/dynamic), 2 years

Configuration management tools

- DesignSync, 8 years
- ClearCase, 10 years
- SubVersion, 1 year

Operating systems

- Windows, Linux, UNIX (Sun, Solaris)

PERSONAL

Nationality:	German
Marital Status:	Single
Date of Birth:	6th of May 1969
Languages:	German (native) English (good) Spanish (basics)
Interests:	Triathlon, digital photography, collecting old records

Date: Feb 2016

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